High Breakdown Voltage, Sub-micron, Strained InGaAlAs/GaAs FET's

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Abstract

Sub-micron gate GaAs FET's with a pseudomorphic surface layer of InGaAlAs used to increase breakdown voltage have been fabricated. A 0.2 μm gate length device with I_{dss} of 360 mA/mm and g_m of 260 mS/mm has a BV_{ds} of 9.3 V and a BV_{gd} of 11.5 V. F_{max} for this device is 80 GHz. The effect upon device performance of gate length, source-to-drain spacing and Al mole fraction was also investigated. The breakdown voltage shows only small changes with changes in gate length at submicron dimensions. The source-to-drain spacing changes not only the breakdown voltage but also appears to change the mechanism that limits high voltage performance.

Introduction

One of the most important mechanisms in the breakdown of a FET is impact ionization in the high field region under the gate. This means that one possible way to increase the breakdown voltage in a FET is to place a material with a low impact ionization rate or high recombination rate under the gate. This idea has been implemented with many materials including insulators [1], wide bandgap semiconductors [2], and low temperature grown semiconductors [3]. Another possible choice as a low impact ionization layer is a pseudomorphic semiconductor. It has been shown that if In is added to GaAs to cause compressive strain, and Al is added to maintain the bandgap of the alloy, the threshold energy for impact ionization in the alloy is dramatically increased [4]. The InGaAlAs alloy, when used as a low impact ionization material under the gate, should provide improved breakdown voltage and better high power performance in a FET.

Fabrication

Devices were fabricated on two wafers to test the effects of a pseudomorphic layer on the performance of a FET. Both wafers were grown by molecular beam epitaxy on semi-insulating GaAs substrates. They both have a GaAs buffer, a 50 nm GaAs channel doped at 5 x 10^{17} /cm^3, and an ohmic cap of GaAs that is 30 nm thick and doped at 6 x 10^{18} /cm^3. Between the channel and the cap is a pseudomorphic layer of InGaAlAs that is 10 nm thick and has no intentional doping. This pseudomorphic layer is $In_{0.2}Ga_{0.62}Al_{0.18}As$, which has a bandgap of about 1.42 eV, in sample 1928 and $In_{0.2}Ga_{0.35}Al_{0.45}As$, which has a bandgap of about 1.8 eV, in sample 1929. Sample 1928 also has an AlAs etch stop layer between the ohmic cap and the pseudomorphic layer.

The FET's on these samples were fabricated by first doing a mesa etch using a $H_3PO_4/H_2O_2/H_2O$ solution. Next Ni/Ge/Au/Ti/Au ohmic contacts were defined by optical lithography, deposited by e-beam evaporation, lifted off, and annealed using a hot plate. The contact resistance, measured by the transmission line method, was around 8.5 x 10^{-7} Ω-cm^2 for both samples.

Gate definition was the last step in the fabrication. The gates were patterned by e-beam lithography and recessed using a $NH_4OH/H_2O_2/H_2O$ etch. The AlAs layer was removed from sample 1928 using a BHF/H_2O solution, and the Ti/Pt/Au gates were deposited on both samples by e-beam evaporation and lifted off. Three different e-beam exposures on each wafer gave gate lengths of 0.15 μm, 0.2 μm, and 0.25 μm. All of these gates were T-gates with equal side-lobe exposures. Both samples have source-drain gaps of 2 μm and 3 μm. The gates are positioned in the center of the source-drain gaps.

Results

The average source-to-drain breakdown voltage for

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25 devices on wafer 1929 with gate lengths of 0.2 μm and source-to-drain spacings of 2 μm is 9.3 V, and the average gate-to-drain breakdown voltage for these same 25 devices is 11.5 V. $BV_{d\text{-}s}$ is defined as the voltage at which the output conductance of the device exceeds 100 mS/mm, and $BV_{d\text{-}g}$ is defined as the voltage at which the gate-to-drain current exceeds 100 μA/mm. The breakdown voltages measured on sample 1929 are significantly higher than the breakdown voltages measured on normal 0.25 μm GaAs MESFET's fabricated and tested by us and on AlGaAs/GaAs HFET's reported by others [5] which are 4 to 6 V $BV_{d\text{-}s}$ and 7 to 9 V $BV_{d\text{-}g}$. The strained layer devices have transconductances greater than 260 mS/mm and current levels above 360 mA/mm. Fig. 1 shows a typical I-V curve for a device on sample 1929.

The high frequency S-parameters of the devices were measured from 0.5 to 24 GHz using on chip probing and an HP8510. From these measurements h_{21} and G_{max} were plotted and extrapolated to find f_t and f_{max}. A typical 0.2 μm gate length device has a f_t of 41 GHz and an f_{max} of 80 GHz.

The effect of the gate length on the performance of the devices was investigated. The frequency performance of the devices improved as the gate length was reduced even though the channel was the same for all devices. F_{max} increased from 74 GHz to 84 GHz as the gate length was reduced from 0.25 μm to 0.15 μm. At the same time the breakdown voltage of the devices, both source-to-drain and gate-to-drain, increased by only 7% as the gate length was increased from 0.15 μm to 0.25 μm. The increase in breakdown voltage as a function of increasing gate length is much greater at longer gate lengths as shown in fig. 2 which includes a 1 μm gate device on a sample with a similar pseudomorphic layer and a similar channel.

The effect of the source-to-drain ohmic metal spacing was also investigated. Both sets of devices have the same gates and the same recess shape since identical gate lithography and channel recessing was done (see fig. 3). The distance from the gate edge to the ohmic cap was measured using SEM analysis and found to be around 0.12 μm for both source-to-drain spacings. It was found that devices with a 3 μm source-to-drain gap had a 30% higher gate-to-drain breakdown voltage than devices with a 2 μm source-to-drain gap. This effect can be explained by the finite resistance of the ohmic cap layer. The resistance per unit length of the ohmic cap on top of the channel is the same for all of the devices. Since the distance from the ohmic metal to the edge of the ohmic cap is longer for the 3 μm gap, the potential at the gate edge of the ohmic cap will be less for 3 μm gap devices than for 2 μm gap devices. Due to this potential difference the depletion region will extend further toward the drain ohmic metal in the 3 μm gap devices. This larger extension leads to reduced electric fields in the depletion region and increased breakdown voltage for the 3 μm gap devices. Other effects from this increased extension that were observed include an increase in the access resistances, a decrease in the output conductance, a decrease in f_t and a slight increase, 2%, in f_{max}.

The size of the source-to-drain gap also affected the characteristics of the breakdown. The smaller source-to-drain gap devices broke down at a high current level, and the device went from breakdown, defined as the voltage at which the device has a high output conductance, to burnout, where device failure is permanent, over a range of 0.2 V to 0.4 V (see fig. 4). The 3 μm source-to-drain gap devices had high output conductance occurring first at high gate-to-drain voltage, near pinchoff (see fig. 5). In these devices the onset of breakdown and device burnout were separated by 1.0 V to 1.5 V. The behavior of the 3 μm gap devices is consistent with a device in which the breakdown is caused by impact ionization in the gate-to-drain region. The breakdown of the 2 μm gap devices, however, is probably not caused solely by impact ionization in the gate-to-drain region since this breakdown does not occur at high gate-to-drain potential but rather at high current levels. This type of breakdown is more typical of a thermal breakdown condition or thermally assisted tunnelling condition [6].

The major limiting factor in these devices is a kink in the drain current, especially near pinchoff (see fig. 2). This limits the pinchoff performance of the devices above a drain-to-source voltage of about 4 V and could severely hurt the high power performance of these devices. Two areas that may be causing the kink are the pseudomorphic layer and the buffer layer. The pseudomorphic layer has a high Al mole fraction which could lead to a high concentration of traps in this layer. To investigate the effect of the high Al mole fraction on the kink we fabricated devices on a sample 1928 which has a much lower Al mole fraction in the strained layer. Fig. 6 shows that the kink, the sudden rise in output conductance, is reduced somewhat with the reduced Al mole fraction. This reduced Al mole

fraction, however, reduces the bandgap and hence the breakdown voltage of the devices. The FET's on sample 1928 with a lower Al mole fraction have a source-to-drain breakdown voltage about 11% lower than those on sample 1929. The change in Al mole fraction seems to have very little effect upon the frequency performance of the device since FET's on sample 1928 and on sample 1929 both have similar high frequency figures of merit.

The other area that may be contributing to the kink is the buffer. Characteristics similar to the kink that we observed have been attributed to the effects of traps in buffer layers [7].

Conclusion

GaAs channel FET's with a pseudomorphic layer of InGaAlAs under the gate have been fabricated. 0.2 µm gate length devices with f_{max} of 80 GHz have a saturation current of 360 mA/mm and a gate-to-drain breakdown voltage of 11.5 V. The power performance of this device is limited by a kink in the pinchoff performance of the device. The kink can be reduced by reducing the Al mole fraction in the pseudomorphic layer but this reduction also reduces the breakdown voltage of the device by reducing the bandgap of the pseudomorphic layer.

The effects of gate length on the performance of the devices were also investigated. It was found that while the breakdown voltage does decrease with decreasing gate length, the reduction is small in the submicron region.

The effects of source-to-drain spacing were also investigated. The breakdown voltage of the device increases as the source-to-drain gap is increased. The source-to-drain spacing also seems to affect the breakdown mechanism in the devices. The devices with larger gaps show impact ionization limited behavior where breakdown occurs first at a high gate-to-drain bias. The devices with smaller gaps have breakdown occurring first at high current, positive gate bias, conditions.

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References

[1] T. Waho and F. Yanagawa, "A GaAs MISFET Using an MBE-Grown CaF_2 Gate Insulator Layer," IEEE Electron Device Lett., vol. 9, no. 10, p. 548, 1988.

[2] H. Hida, A. Okllamoto, H. Toyoshima and K. Ohata, "A High-Current Drivability i-AlGaAs/n-GaAs Doped-Channel MIS-like FET (DMT)," IEEE Electron Device Lett., vol. EDL-7, no. 11, p. 625, 1986.

[3] L. W. Yin, Y. Hwang, J. H. Lee, R. M. Kolbas, R. J. Trew and U. K.Mishra, "Improved Breakdown Voltage in GaAs MESFET's Utilizing Surface Layers of GaAs Grown at a Low Temperature by MBE," IEEE Electron Device Lett., vol. 11, no. 12, p. 561, 1990.

[4] J. Singh, "A Theoretical Study of Electron Impact Ionisation in Pseudomorphic InGaAlAs on GaAs and InP Substrates," Presented at the 1991 International Symposium on Gallium Arsenide and Related Compounds, Sept. 23-26, 1991.

[5] A.I. Akinwande, K.L. Tan, C.H. Chen, P.J. Vold, "A Self-Aligned Gate Lightly Doped Drain (Al,Ga)As/GaAs MODFET," IEEE Electron Device Lett., vol. 9, no. 6, p. 275, 1988.

[6] R.J. Trew and U.K. Mishra, "Gate Breakdown in MESFET's and HEMT's," IEEE Electron Device Lett., vol. 12, no. 10, p. 524, 1991.

[7] S. Tehrani, H. Boronkin, M.M. Hoogstra, G.N. Maracas, J.A. Curless, G.D. Kramer, M.S. Peffley, and R.K. Tsui, "Excess Drain Current in Heterojunction FET's due to Substrate Space-Charge-Limited Current," IEEE Trans. on Electron Devices, vol. 36, no. 9, p. 1591, 1989.

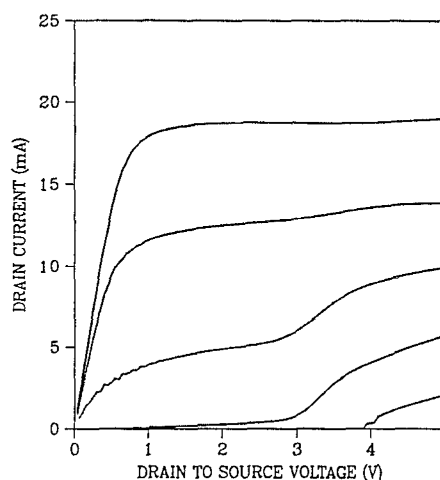

Figure 1. Typical I-V curve for a FET on sample 1929. Gate length is 0.2 µm and gate width is 50 µm. Maximum gate voltage is 0.5 V and step size is -0.5 V.

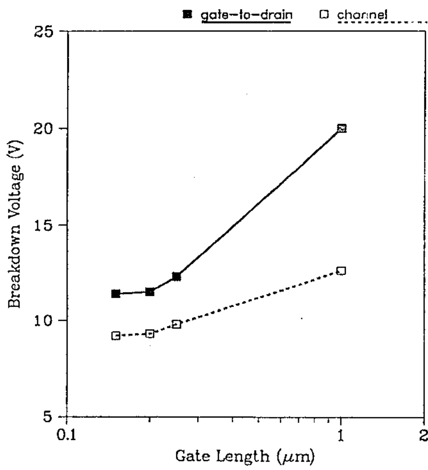

Figure 2. Breakdown voltage vs. gate length. Upper curve is gate-to-drain breakdown, lower curve is source-to-drain breakdown.

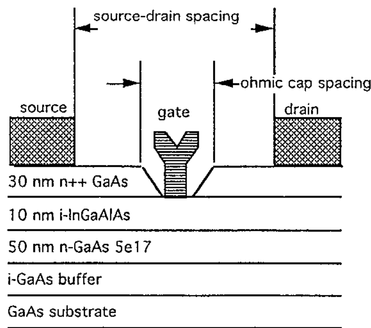

Figure 3. Schematic drawing of a cross-section of a FET on sample 1929.

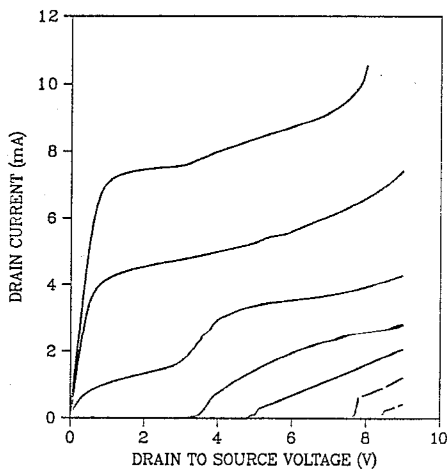

Figure 4. I-V curve for a FET on sample 1929. Gate length is 0.2 µm, source-to-drain ohmic metal spacing is 2 µm, and gate width is 30 µm. Maximum gate voltage is 0.5 V and step size is -0.5 V.

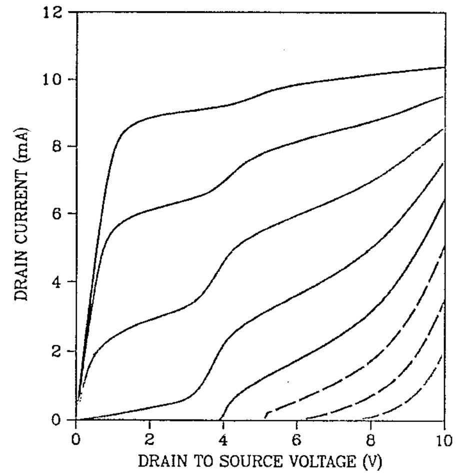

Figure 5. I-V curve for a FET on sample 1929. Gate length is 0.2 µm, source-to-drain ohmic metal spacing is 3 µm, and gate width is 30 µm. Maximum gate voltage is 0.5 V and step size is -0.5 V.

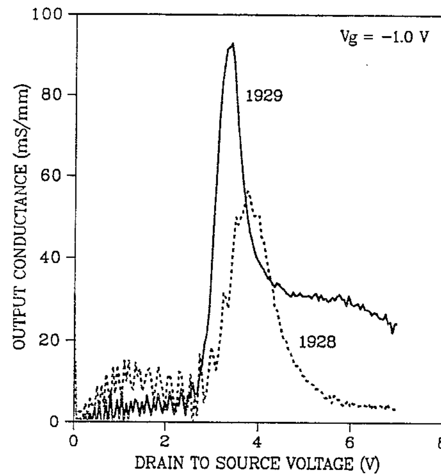

Figure 6. Output conductance vs. drain bias for FET's on samples 1928 and 1929. Gate voltage is -1.0 V.